FAIRCHILD SEMICONDUCTOR™

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MM74C911
4-Digit Expandable Segment Display Controller

General Description

The MM74C911 display controller is an interface element with memory that drives a 4-digit, 8-segment LED display. The MM74C911 allows individual control of any segment in the 4-digit display. The number of segments per digit can be expanded without any external components. For example, two MM74C911's can be cascaded to drive a 16-segment alpha-numeric display.

The display controllers receive data information through 8 data lines a, b…DP, and digit information through 2 address inputs K1 and K2. The input data is written into the register selected by the address information when $\overline{\text{CHIP ENABLE}}$, $\overline{\text{CE}}$, and $\overline{\text{WRITE ENABLE}}$, $\overline{\text{WE}}$, are LOW and is latched when either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ return HIGH. Data hold time is not required.

A self-contained internal oscillator sequentially presents the stored data to high drive (100 mA typ.) 3-STATE output drivers which directly drive the LED display. The drivers are active when the control pin labeled $\overline{\text{SEGMENT OUTPUT ENABLE}}$, $\overline{\text{SOE}}$, is LOW and go into 3-STATE when $\overline{\text{SOE}}$ is HIGH. This feature allows for duty cycle brightness control, or for disabling the output drive for power conservation.

The digit outputs directly drive the base of the digit transistor when the control pin labeled $\overline{\text{DIGIT INPUT OUTPUT}}$, $\overline{\text{DIO}}$, is LOW. When $\overline{\text{DIO}}$ is HIGH, the digit lines turn into inputs and the internal scanning multiplexer is disabled.

When any digit line is forced HIGH by an external device, usually another MM74C911, the data information for that digit is presented to the output. In this manner, 16-segment alpha-numeric displays, 24- or 32-segment displays, or an array of discrete LED's can be controlled by the simple cascading of expandable segment display controllers. All inputs except digit inputs are TTL compatible and do not clamp input voltages above V_{CC}.

Features

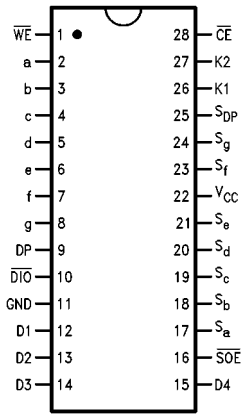
- Direct segment drive (100 mA typ.) 3-STATE
- 4 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor
- Segment expandability without external components
- TTL compatible inputs
- Power saver mode—5 μW (typ.)

Ordering Code:

Order Number	Package Number	Package Description
MM74C991N	N28B	28-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS–010, 0.600" Wide

Connection Diagram

Pin Assignments for DIP



Top View

Truth Tables

Input Control

$\overline{CE}$	Digit Address		$\overline{WE}$	Operation
	K2	K1		
0	0	0	0	Write Digit 1
0	0	0	1	Latch Digit 1
0	0	1	0	Write Digit 2
0	0	1	1	Latch Digit 2
0	1	0	0	Write Digit 3
0	1	0	1	Latch Digit 3
0	1	1	0	Write Digit 4
0	1	1	1	Latch Digit 4
1	X	X	X	Disable Writing

Output Control

$\overline{DIO}$	$\overline{SOE}$	Digit Lines				Operation
		D4	D3	D2	D1	
0	0	R	R	R	R	Refresh Display
0	1	R	R	R	R	Disable Segment Outputs
1	0	0	0	0	0	Digits Are Now Inputs
1	0	0	0	0	1	Display Digit 1
1	0	0	0	1	0	Display Digit 2
1	0	0	1	0	0	Display Digit 3
1	0	1	0	0	0	Display Digit 4
1	1	0	0	0	0	Power Saver Mode

R = Refresh (digit lines sequentially pulsed)
X = Don't Care

Functional Description

The MM74C911 display controller is manufactured on standard metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin to suppress current transients.

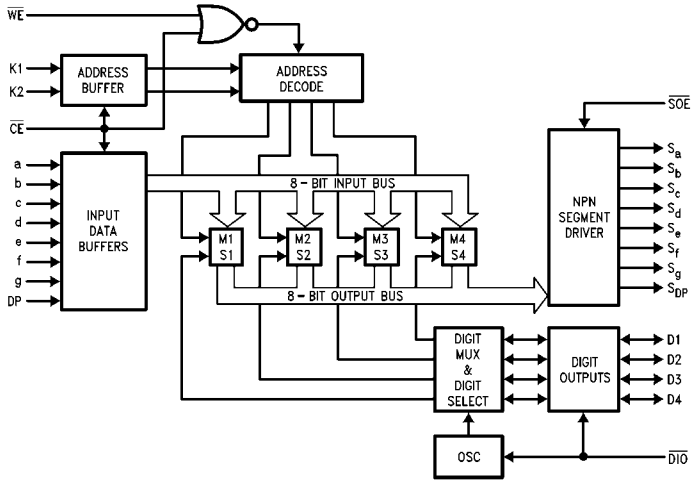
The digit outputs directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration. If an MM74C911 is driving a digit transistor and also supplying digit information to a cascaded MM74C911, base resistors are needed in the digit transistors to provide an adequate high level to the digit inputs of the cascaded MM74C911.

As seen in the Block Diagram, these display controllers contain four 8-bit registers; any one may be randomly written into. In normal operation, the internal multiplexer scans the registers and refreshes the display. In cascaded operation, 1 MM74C911 serves as a master refresh device and cascaded MM74C911's are slaved to it through digit lines operating as inputs.

The MM74C911 appears to a microprocessor as memory and to the user as a self-scan display. Since every segment is under microprocessor control, great versatility is obtained.

Low power standby operation occurs with both $\overline{SOE}$ and $\overline{DIO}$ inputs HIGH. This condition forces the MM74C911 to a quiescent state typically drawing less than 1 μA of supply current with a standby supply voltage as low as 3V.

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Voltage at Any Pin except Inputs	−0.3V to V_{CC} + 0.3V
Voltage at Any Input except Digits	−0.3V to +15V
Operating Temperature Range, (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltage reference to ground.

DC Electrical Characteristics

Min/Max limits apply at −40°C ≤ T_J ≤ +85°C, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5V, V_{IN} = 0V	−1.0	−0.005		µA
I_{CC}	Supply Current (Normal)	V_{CC} = 5V, Outputs Open		0.50	2.5	mA
I_{CC}	Supply Current (Power Saver)	V_{CC} = 5V, $\overline{SOE}$, $\overline{DIO}$ = "1", D1, D2, D3, D4 = "0"		1	600	µA
I_{OUT}	3-STATE Output Current	V_O = 5V		0.03	10	µA
		V_O = 0V	−10	−0.03		
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 2			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE						
I_{SH}	HIGH Level Segment Current	V_{CC} = 5V, V_O = 3.4V				
		T_J = 25°C	−60	−100		mA
		T_J = 100°C	−40	−60		mA
I_{DH}	HIGH Level Digit Current	V_{CC} = 5V, V_O = 3V				
		T_J = 25°C	−10	−20		mA
		T_J = 100°C	−7	−10		mA
		V_{CC} = 5V, V_O = 1V				
		T_J = 25°C	−15	−40		mA
		T_J = 100°C	−10	−15		mA
$V_{OUT(1)}$	Logical "1" Output Voltage, Any Digit	V_{CC} = 5V, I_O = −360 µA	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage, Any Output	V_{CC} = 5V, I_O = 360 µA			0.4	V
θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 3: θ_{JA} measured in free-air with device soldered into printed circuit board.

AC Electrical Characteristics (Note 4)

V_{CC} = 5V, $t_r = t_f$ = 20 ns, C_L = 50 pF

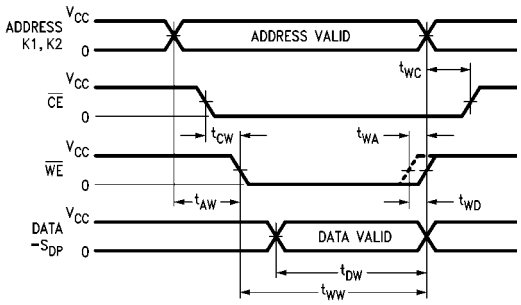
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CW}	Chip Enable to Write Enable Set-Up Time	T_J = 25°C	35	15		ns
		T_J = 125°C	50	20		ns
t_{AW}	Address to Write Enable Set-Up Time	T_J = 25°C	35	15		ns
		T_J = 125°C	50	20		ns
t_{WW}	Write Enable Width	T_J = 25°C	400	225		ns
		T_J = 125°C	450	250		ns
t_{DW}	Data to Write Enable Set-Up Time	T_J = 25°C	390	225		ns
		T_J = 125°C	430	250		ns
t_{WD}	Write Enable to Data Hold Time	T_J = 25°C	0	−10		ns
		T_J = 125°C	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	T_J = 25°C	0	−10		ns
		T_J = 125°C	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	T_J = 25°C	55	30		ns
		T_J = 125°C	75	40		ns
t_{1H}, t_{0H}	Logical “1”, Logical “0” Levels into 3-STATE	R_L=10k, C_L=10 pF				
		T_J = 25°C		275	500	ns
		T_J = 125°C		325	600	ns
t_{H1}, t_{H0}	3-STATE to Logical “1” or	R_L=10k, C_L=10 pF				
	Logical “0” Levels	T_J = 25°C		325	600	ns
		T_J = 125°C		375	700	ns
t_{D1}, t_{D0}	Propagation Delay from Digit Input to	T_J = 25°C		500	1000	ns
	Segment Output	T_J = 125°C		700	1400	ns
t_{IB}	Interdigit Blanking Time	T_J = 25°C	5	10		µs
		T_J = 125°C	10	20		µs
f_{MUX}	Multiplex Scan Frequency	T_J = 25°C		525		Hz
		T_J = 125°C		375		Hz
C_{IN}	Input Capacitance	(Note 5)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	(Note 5)		30	50	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

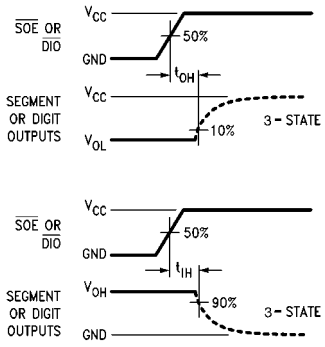
Note 5: Capacitance guaranteed by periodic testing.

Switching Time Waveforms

Write Data Waveforms

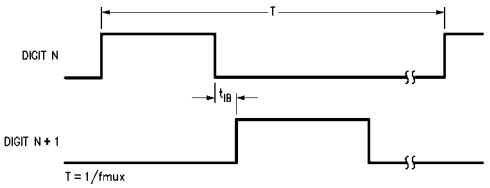


3-STATE Waveforms

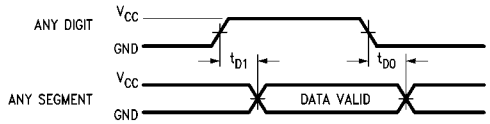


Switching Time Waveforms (Continued)

Multiplexing Output Waveforms

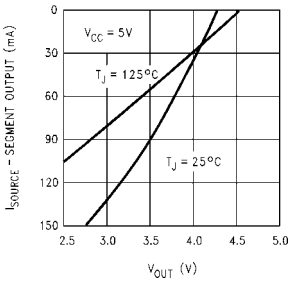


Read Data Waveforms

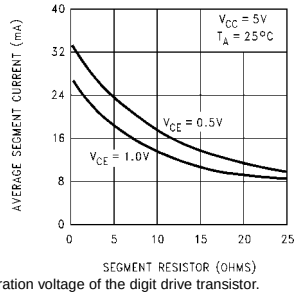


Note A: All other digit lines are at a low level. $\overline{DIO}$ at a HIGH level.

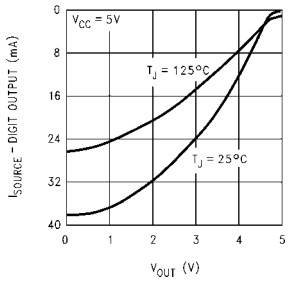
Typical Performance Characteristics



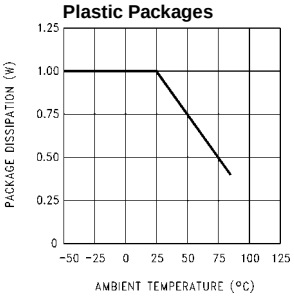
Segment outputs if shorted to ground will exceed maximum power dissipation of the device.



V_{CE} is the saturation voltage of the digit drive transistor.

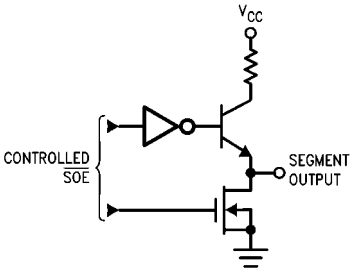


Power Dissipation vs Temperature for Plastic Packages

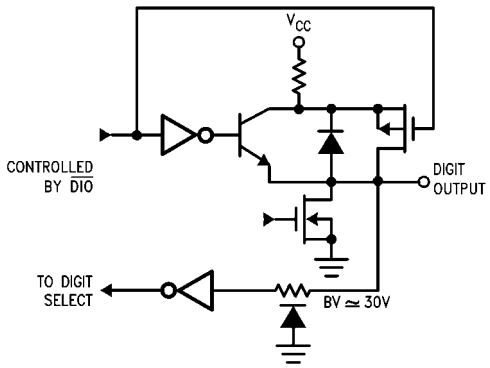


Applications

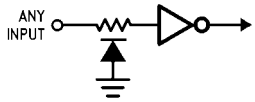
Segment Output Structure



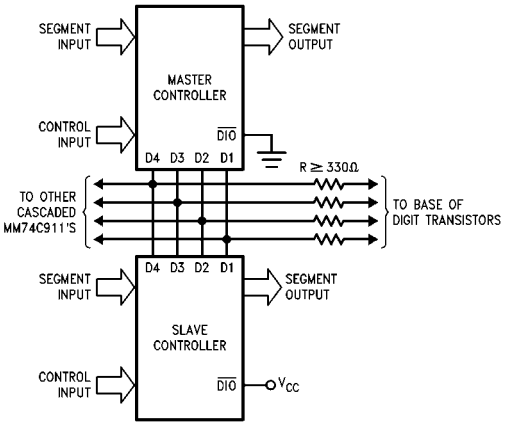
Digit Output Structure



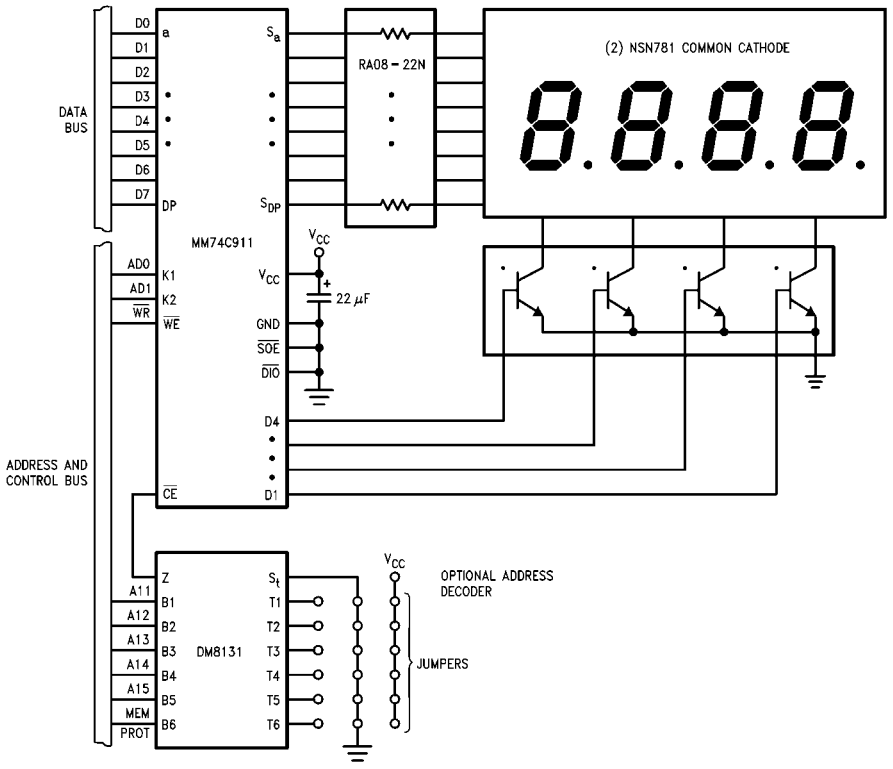
Input Protection



Segment Expansion

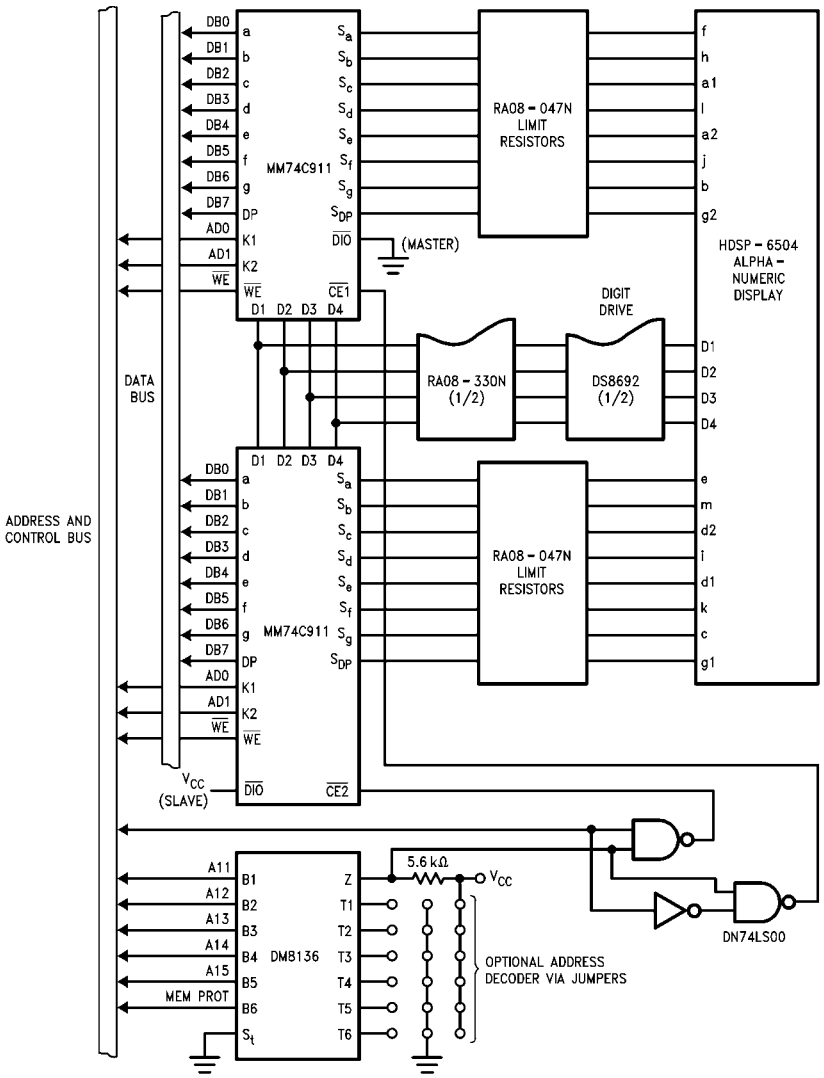


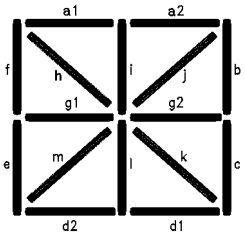
Typical Application



*Base resistors may be necessary to limit base current.

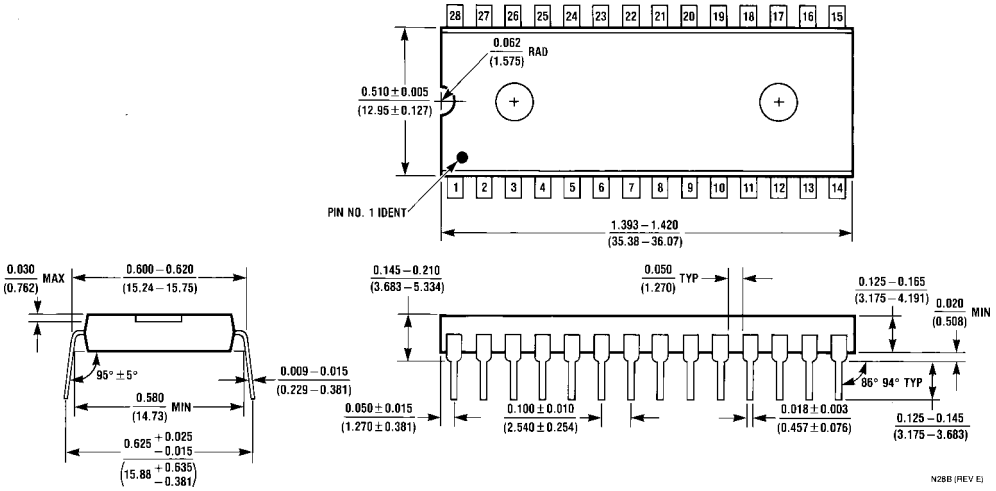
4-Digit, 16-Segment Alpha-Numeric Display





Segment Identification

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
Package Number N28B